

WHAT IS CLAIMED IS:

- 1 1. An apparatus for receiving a non-coherent layered modulation signal,
2 comprising:
3 a tuner for receiving a layered signal and producing a layered in-phase signal
4 and a layered quadrature signal therefrom;
5 an analog-to-digital converter for digitizing the layered in-phase signal and the
6 layered quadrature signal;
7 a processor for decoding the layered in-phase signal and the layered
8 quadrature signal to produce a single layer in-phase signal and a single layer
9 quadrature signal;
10 a digital-to-analog encoder for converting the single layer in-phase signal and
11 the single layer quadrature signal to a single layer in-phase analog signal and a single
12 layer quadrature analog signal; and
13 a modulator for modulating the single layer in-phase analog signal and the
14 single layer quadrature analog signal to produce a single layer signal.
- 1 2. The apparatus of Claim 1, wherein the layered signal is compatible
2 with a legacy receiver such that at least one signal layer is decodeable directly from
3 the layered signal with the legacy receiver.
- 1 3. The apparatus of Claim 1, wherein the single layer signal from the
2 modulator is decodeable with a legacy receiver.
- 1 4. The apparatus of Claim 1, wherein the processor comprises a logic
2 circuit.

1 5. The apparatus of Claim 1, wherein decoding by the processor
2 comprises match filtering the layered in-phase signal and the layered quadrature
3 signal.

1 6. The apparatus of Claim 1, wherein the processor demodulates and
2 decodes an upper layer signal from the layered in-phase signal and the layered
3 quadrature signal.

1 7. The apparatus of Claim 6, wherein the processor produces an ideal
2 upper layer signal including an ideal in-phase upper layer signal and an ideal
3 quadrature upper layer signal from the decoded upper layer signal and subtracts the
4 ideal in-phase upper layer signal and the ideal quadrature upper layer signal from the
5 layered in-phase signal and the layered quadrature signal, respectively, to produce the
6 single layer in-phase signal and the single layer quadrature signal.

1 8. The apparatus of Claim 7, wherein the layered in-phase signal and the
2 layered quadrature signal are delayed to synchronize the subtraction.

1 9. The apparatus of Claim 7, wherein producing the ideal upper layer
2 signal comprises signal processing the ideal in-phase upper layer signal and the ideal
3 quadrature upper layer signal.

1 10. The apparatus of Claim 9, wherein signal processing the ideal in-phase
2 upper layer signal and the ideal quadrature upper layer signal comprises finite impulse
3 response matched filtering the ideal in-phase upper layer signal and the ideal
4 quadrature upper layer signal.

1 11. The apparatus of Claim 9, wherein signal processing the ideal in-phase
2 upper layer signal and the ideal quadrature upper layer signal comprises applying a
3 signal map to the ideal in-phase upper layer signal and the ideal quadrature upper
4 layer signal, the signal map accounting for transmission distortions of the layered
5 signal.

1 12. The apparatus of Claim 9, wherein signal processing the ideal in-phase
2 upper layer signal and the ideal quadrature upper layer signal comprises amplitude
3 and phase matching the ideal in-phase upper layer signal and the ideal quadrature
4 upper layer signal with the layered in-phase signal and the layered quadrature signal,
5 respectively.

1 13. A digital processor for decoding a layered signal to produce a single
2 layer signal, comprising:
3 a demodulator and decoder for decoding an upper layer signal from the layered
4 signal;
5 an encoder for generating an ideal upper layer signal from the decoded upper
6 layer signal;
7 a signal processor for modifying the ideal upper layer signal to characterize
8 transmission and processing effects; and
9 a subtractor for subtracting the modified ideal upper layer signal from the
10 layered signal to produce the single layer signal.

1 14. The digital processor of Claim 13, further comprising a delay function
2 correlated to an output of the signal processor to appropriately delay the layered signal
3 to synchronize amplitude and phase matching of the modified ideal upper layer signal
4 and the layered signal.

1 15. The digital processor of Claim 13, further comprising a delay function
2 correlated to an output of the signal processor to appropriately delay the layered signal
3 to synchronize subtraction of the modified ideal upper layer signal and the layered
4 signal.

1 16. The digital processor of Claim 13, wherein the signal processor
2 performs finite impulse response matched filtering on the ideal upper layer signal.

1 17. The digital processor of Claim 13, wherein the signal processor
2 applies a signal map to the ideal upper layer signal.

1 18. The digital processor of Claim 13, wherein the signal processor
2 amplitude and phase matches the ideal upper layer signal with the layered signal.

1 19. A method of receiving a non-coherent layered modulation signal,
2 comprising the steps of:
3 receiving a layered signal and producing a layered in-phase signal and a
4 layered quadrature signal therefrom;
5 digitizing the layered in-phase signal and the layered quadrature signal;
6 decoding the layered in-phase signal and the layered quadrature signal to
7 produce a single layer in-phase signal and a single layer quadrature signal;
8 converting the single layer in-phase signal and the single layer quadrature
9 signal to a single layer in-phase analog signal and a single layer quadrature analog
10 signal; and
11 modulating the single layer in-phase analog signal and the single layer
12 quadrature analog signal to produce a single layer signal.

1 20. The method of Claim 19, wherein the layered signal is compatible with
2 a legacy receiver such that at least one signal layer is decodeable directly from the
3 layered signal with the legacy receiver.

1 21. The method of Claim 19, wherein the single layer signal from the
2 modulator is decodeable with a legacy receiver.

1 22. The method of Claim 19, wherein the step of decoding is performed by
2 a logic circuit.

1 23. The method of Claim 19, wherein the step of decoding comprises
2 match filtering the layered in-phase signal and the layered quadrature signal.

1 24. The method of Claim 19, wherein the step of decoding comprises
2 demodulating and decoding an upper layer signal from the layered in-phase signal and
3 the layered quadrature signal.

1 25. The method of Claim 24, wherein the step of decoding comprises
2 producing an ideal upper layer signal including an ideal in-phase upper layer signal
3 and an ideal quadrature upper layer signal from the decoded upper layer signal and
4 subtracting the ideal in-phase upper layer signal and the ideal quadrature upper layer
5 signal from the layered in-phase signal and the layered quadrature signal, respectively,
6 to produce the single layer in-phase signal and the single layer quadrature signal.

1 26. The method of Claim 25, wherein the step of decoding further
2 comprises delaying the layered in-phase signal and the layered quadrature signal to
3 synchronize the subtraction.

1 27. The method of Claim 25, wherein producing the ideal upper layer
2 signal comprises signal processing the ideal in-phase upper layer signal and the ideal
3 quadrature upper layer signal.

1 28. The method of Claim 27, wherein signal processing the ideal in-phase
2 upper layer signal and the ideal quadrature upper layer signal comprises finite impulse
3 response matched filtering the ideal in-phase upper layer signal and the ideal
4 quadrature upper layer signal.

1 29. The method of Claim 27, wherein signal processing the ideal in-phase
2 upper layer signal and the ideal quadrature upper layer signal comprises applying a
3 signal map to the ideal in-phase upper layer signal and the ideal quadrature upper
4 layer signal, the signal map accounting for transmission distortions of the layered
5 signal.

1 30. The method of Claim 27, wherein signal processing the ideal in-phase
2 upper layer signal and the ideal quadrature upper layer signal comprises amplitude
3 and phase matching the ideal in-phase upper layer signal and the ideal quadrature
4 upper layer signal with the layered in-phase signal and the layered quadrature signal,
5 respectively.